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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT251
8-input multiplexer; 3-state

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

8-input multiplexer; 3-state 74HC/HCT251

FEATURES

- True and complement outputs
- Both outputs are 3-state for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT251 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT251 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S_0, S_1, S_2) controlling the switch positions. Assertion (Y) and negation ($\overline{Y}$) outputs are both provided. The output enable input ($\overline{OE}$) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \overline{OE}.(I_0.\overline{S}_0.\overline{S}_1.\overline{S}_2 + I_1.S_0.\overline{S}_1.\overline{S}_2 + I_2.\overline{S}_0.S_1.\overline{S}_2 + I_3.S_0.S_1.\overline{S}_2 + I_4.\overline{S}_0.\overline{S}_1.S_2 + I_5.S_0.\overline{S}_1.S_2 + I_6.\overline{S}_0.S_1.S_2 + I_7.S_0.S_1.S_2)$$

Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	I_n to Y		15	19	ns
	I_n to $\overline{Y}$		17	19	ns
	S_n to Y		20	20	ns
	S_n to $\overline{Y}$		21	21	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	$\overline{Y}$	complementary multiplexer output
7	$\overline{OE}$	3-state output enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage

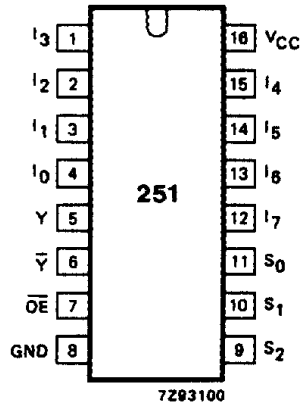

Fig.1 Pin configuration.

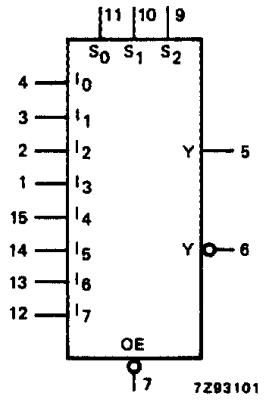

Fig.2 Logic symbol.

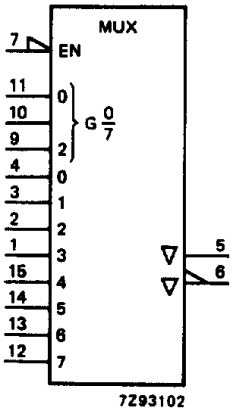

Fig.3 IEC logic symbol.

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

Note

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   Z = high impedance OFF-state

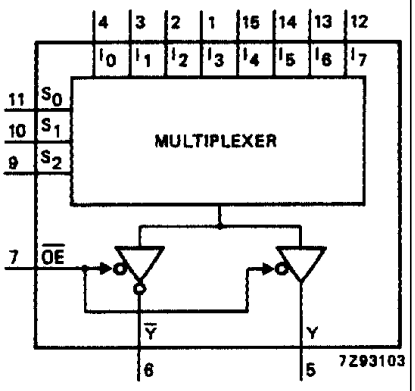

Fig.4 Functional diagram.

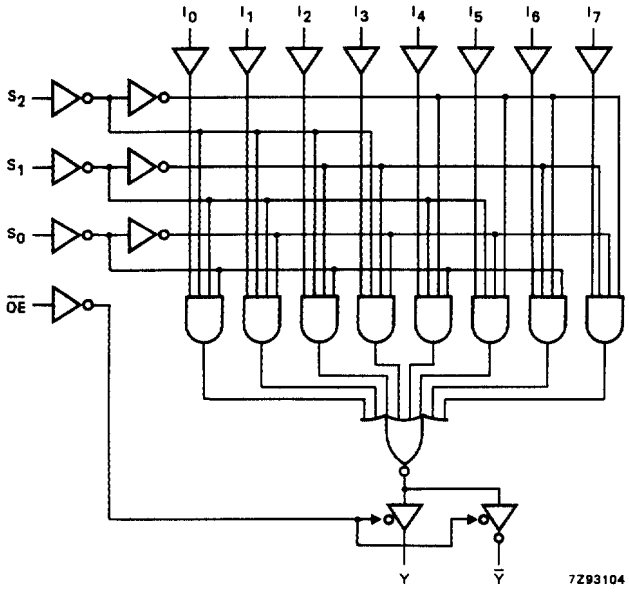

Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay I_n to Y		50 18 14	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay I_n to $\overline{Y}$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay S_n to Y		66 24 19	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay S_n to $\overline{Y}$		69 25 20	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to Y, $\overline{Y}$		36 13 10	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to Y, $\overline{Y}$		39 14 11	140 28 24		170 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I_n	1.00
S_0	1.50
S_1, S_2	1.50
$\overline{OE}$	1.50

AC CHARACTERISTICS FOR HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay I_n to Y		22	35		44		53	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay I_n to $\overline{Y}$		22	35		44		53	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay S_n to Y		24	44		55		66	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay S_n to $\overline{Y}$		25	44		55		66	ns	4.5	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to Y, $\overline{Y}$		13	28		35		42	ns	4.5	Fig.7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to Y, $\overline{Y}$		14	28		35		42	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3V; V_I = GND to 3 V.

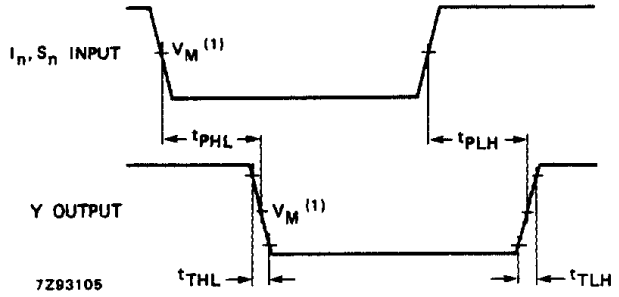

Fig.6 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output (Y) propagation delays and the output transition times.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3V; V_I = GND to 3 V.

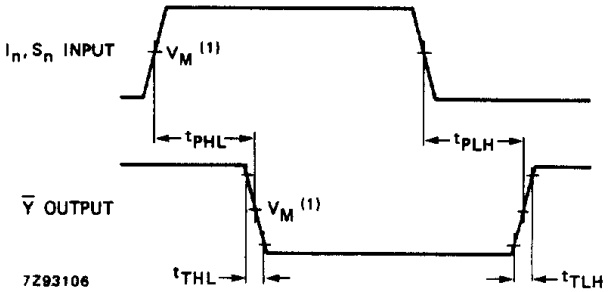

Fig.7 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output ($\overline{Y}$) propagation delays and the output transition times.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3V; V_I = GND to 3 V.

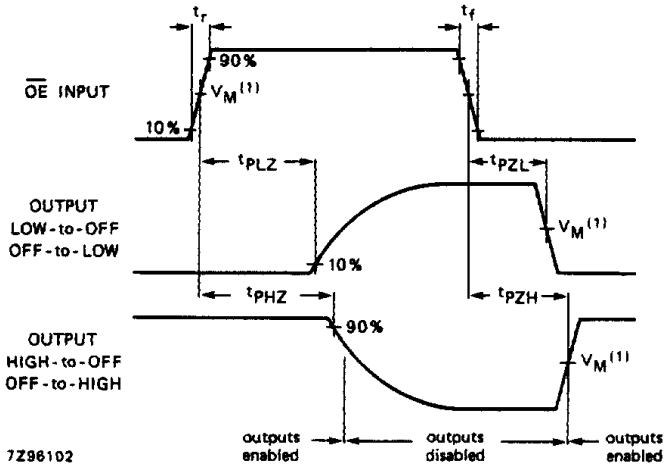

Fig.8 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.